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Search Results -

Term	Documents
(36 AND 33).PGPB,USPT.	3
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side by side		
<i>DB=PGPB,USPT; PLUR=YES; OP=OR</i>		
<u>L37</u> L36 and l33	3	<u>L37</u>
<u>L36</u> (711/213-221)![CCLS]	2192	<u>L36</u>
<i>DB=PGPB,USPT,USOC,EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR</i>		
<u>L35</u> L33 and l28	53	<u>L35</u>
<u>L34</u> L33 and l27	157	<u>L34</u>
<u>L33</u> L32 and decod\$5	185	<u>L33</u>
<u>L32</u> L31 and superscal\$5	190	<u>L32</u>
<u>L31</u> l26 and retir\$7	284	<u>L31</u>
<i>DB=PGPB,USPT; PLUR=YES; OP=OR</i>		
<u>L30</u> l26 and l27	552	<u>L30</u>
<u>L29</u> (712/23,24, 205-219, 225-248)[CCLS]	927	<u>L29</u>

<u>L28</u>	(712/23,24, 205-219, 225-248)! [CCLS]	927	<u>L28</u>
<u>L27</u>	(712/2-300)[CCLS]	11905	<u>L27</u>
<i>DB=PGPB,USPT,USOC,EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR</i>			
<u>L26</u>	L25 and l24	670	<u>L26</u>
<u>L25</u>	(concurrent\$3 or simultaneous\$3 or parallel\$6 or pipelin\$5)	5181998	<u>L25</u>
<u>L24</u>	L22 and (speculativ\$6 or predict\$5)	676	<u>L24</u>
<u>L23</u>	L22 and predict\$5	666	<u>L23</u>
<u>L22</u>	L21 and branch near7 taken	823	<u>L22</u>
<u>L21</u>	l19 and instruction near1 buffer	2647	<u>L21</u>
<u>L20</u>	dependen\$6 and 11	1	<u>L20</u>
<u>L19</u>	(identif\$5 or indicat\$5 or determin\$3) near8 (order or sequenc\$3 or branch\$3 or stream\$1)	680872	<u>L19</u>
<u>L18</u>	4200927.pn. and retir\$7	0	<u>L18</u>
<u>L17</u>	l15 and retir\$7	11	<u>L17</u>
<u>L16</u>	retir\$7 and 11	0	<u>L16</u>
<u>L15</u>	l13 not l14	79	<u>L15</u>
<u>L14</u>	L13 and superscala\$3	55	<u>L14</u>
<u>L13</u>	L12 and predict\$3	134	<u>L13</u>
<u>L12</u>	detect\$3 near5 conditional near1 branch	292	<u>L12</u>
<i>DB=USPT; PLUR=YES; OP=OR</i>			
<u>L11</u>	L9 and branch\$3	1	<u>L11</u>
<u>L10</u>	L9 and detect\$3	0	<u>L10</u>
<u>L9</u>	3718912.pn.	1	<u>L9</u>
<u>L8</u>	L7 and superscalar	1	<u>L8</u>
<u>L7</u>	L6 and 15	1	<u>L7</u>
<u>L6</u>	(identif\$5 or indicat\$5 or determin\$3) near8 (order or sequenc\$3 or branch\$3 or stream\$1)	341178	<u>L6</u>
<u>L5</u>	L4 and taken	1	<u>L5</u>
<u>L4</u>	L3 and (cancel\$5 or suspend\$3)	1	<u>L4</u>
<u>L3</u>	L2 and predict\$5	1	<u>L3</u>
<u>L2</u>	L1 and branch	1	<u>L2</u>
<u>L1</u>	5488729.pn.	1	<u>L1</u>

END OF SEARCH HISTORY

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IEE JNL IEE Journal or Magazine

IEEE CNF IEEE Conference Proceeding

IEE CNF IEE Conference Proceeding

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Zhu, Y.; Wong, W.F.;

[High Performance Computing in the Asia-Pacific Region, 2000, Proceedings, The Fourth International Conference/Exhibition on](#)

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Modeling architectural improvements in superscalar processors

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Abstract

A model of **superscalar** processors using a network of Multiple-Class-Multiple-Resource queues is described and studied. The model is able to model and study instruction classes, instruction dependencies, the cache, the **branch** unit, the **decoder** unit, the **instruction buffer**, the functional units, the retirement buffer, the retirement unit and instruction issue policy in an integrated manner. The model has been verified against measured performance and has shown an average error of 5%

Index Terms**Inspec****Controlled Indexing**[buffer storage](#) [computer architecture](#) [instruction sets](#) [performance evaluation](#) [queueing theory](#)**Non-controlled Indexing**[Multiple-Class-Multiple-Resource queues](#) [architectural improvement modeling](#) [average error](#) [branch unit](#) [central instruction buffer](#) [decoder unit](#) [functional units](#) [instruction classes](#) [instruction dependencies](#) [issue policy](#) [measured performance](#) [retirement buffer](#) [retirement unit](#) [superscalar processors](#)**Author Keywords**

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